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(54) FLOATING GATE NON-VOLATILE MEMORY DEVICE, AND A METHOD OF MANUFACTURING THE DEVICE

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(57) The invention relates in particular, though not exclusively, to an integrated circuit with an embedded non-volatile memory with floating gate (10). According to the invention, at least two poly layers of equal or at least substantially equal thickness are used for this device. The first poly layer, poly A, is for the floating gate (10) and for the gates (22) of NMOS and PMOS in the logic portion of the circuit. The second poly layer, poly B, serves exclusively for the control electrode (21) above the floating gate. If so desired, a third poly layer may be deposited for both the control electrode and the logic gates, so that the thickness of these electrodes, and thus their resistances, are given desired values. Problems like overetching and bridging during saliciding are prevented in that the control electrode and the logic gates have the same thickness.